CMS Upgrade

and its impact on Flavour Physics

Motivations

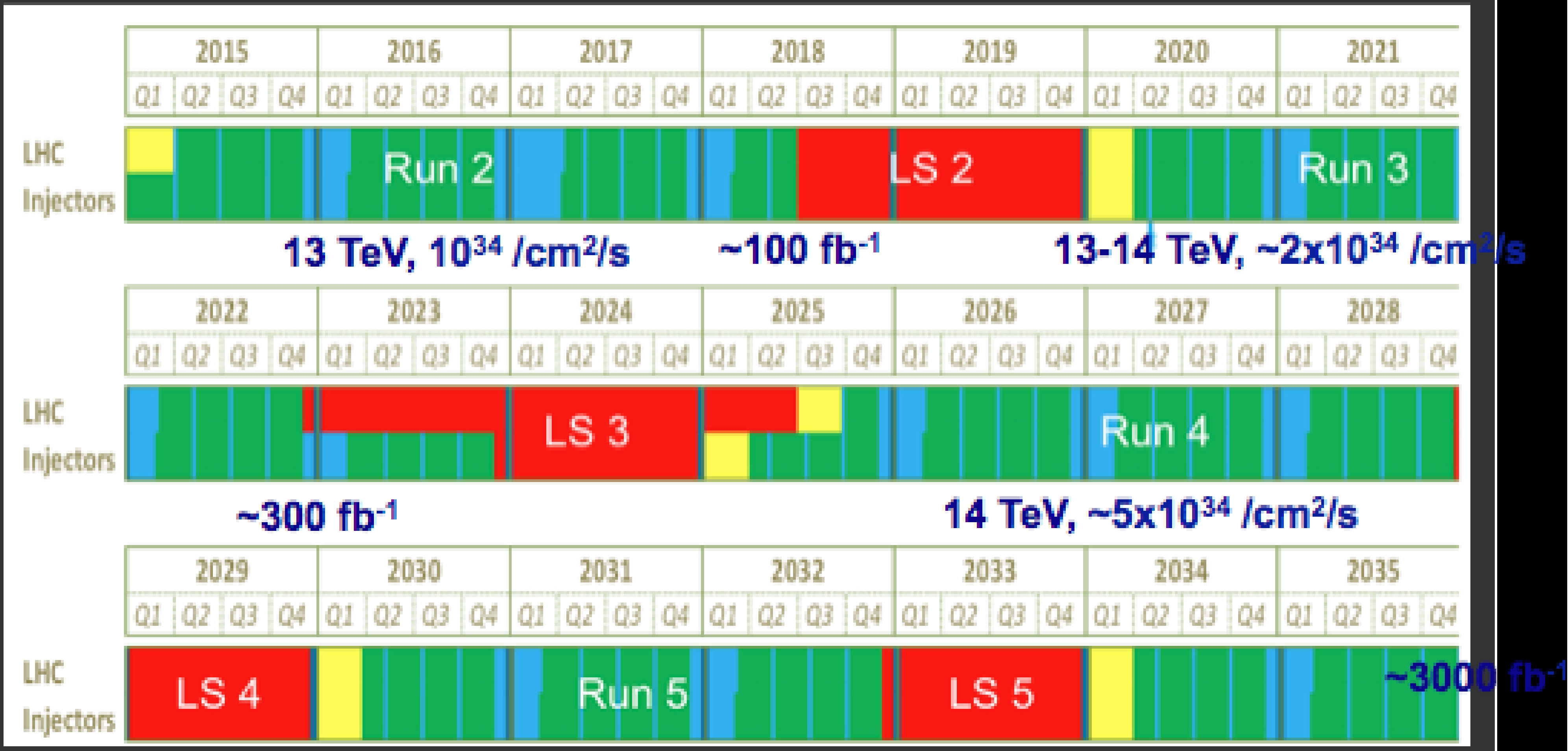
- LHC will undergo sizeable upgrades in the near and in longer terms
  - Luminosity increase
  - Pile-up and Background increase

Increased trigger rate and data-event size

- Purpose of CMS upgrades :
  - maintain / improve wrt present performances, despite the more difficult operating conditions
  - ensure radiation resistance, and easy replacements during short shutdown
- Major and minor interventions
  - mostly aimed at High-p_T Physics
  - beneficent for B-Physics as well

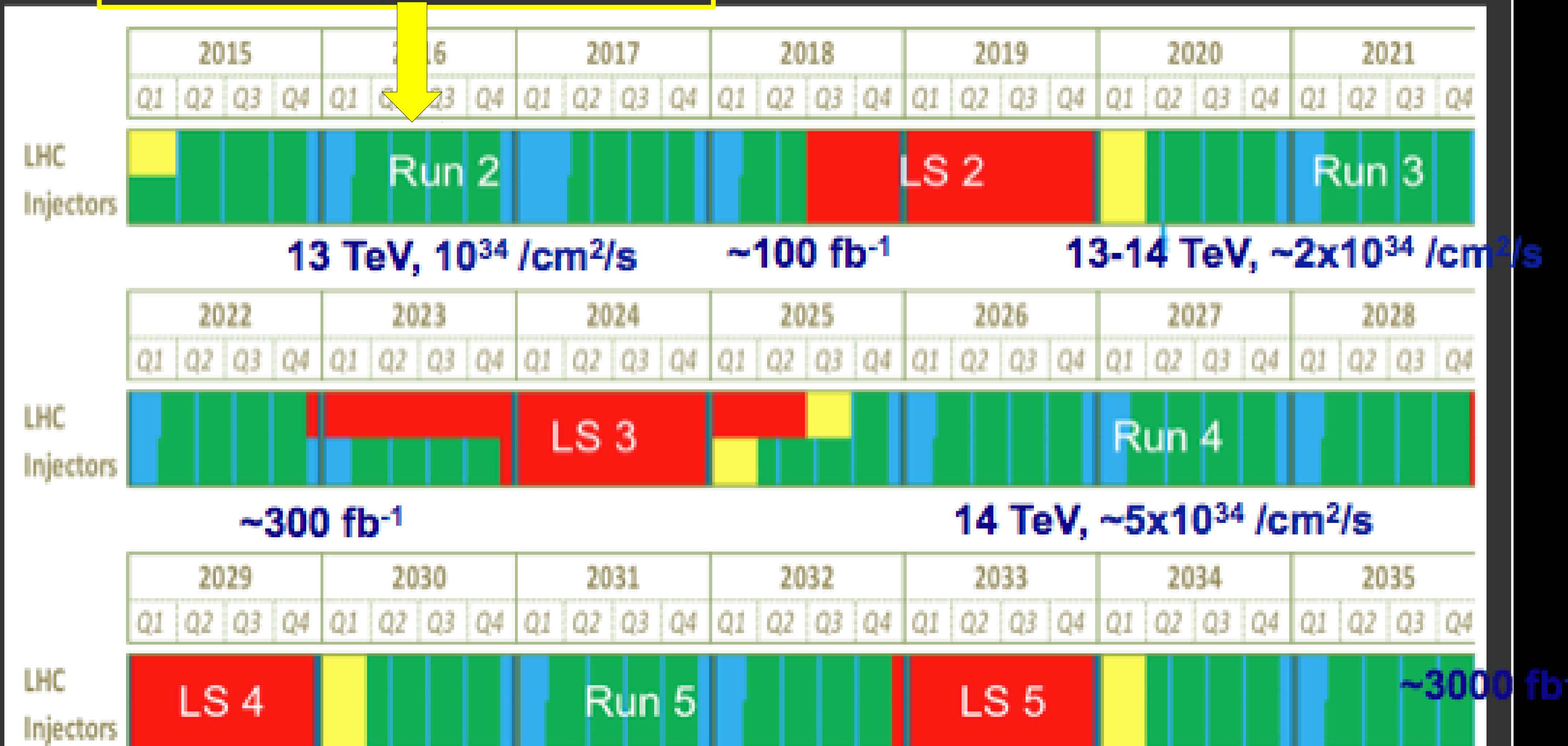
FOCUS for this talk

Upgrade Plan



Upgrade Plan

2015 : RUN with smaller beam pipe, useful for next upgrade



Upgrade Plan

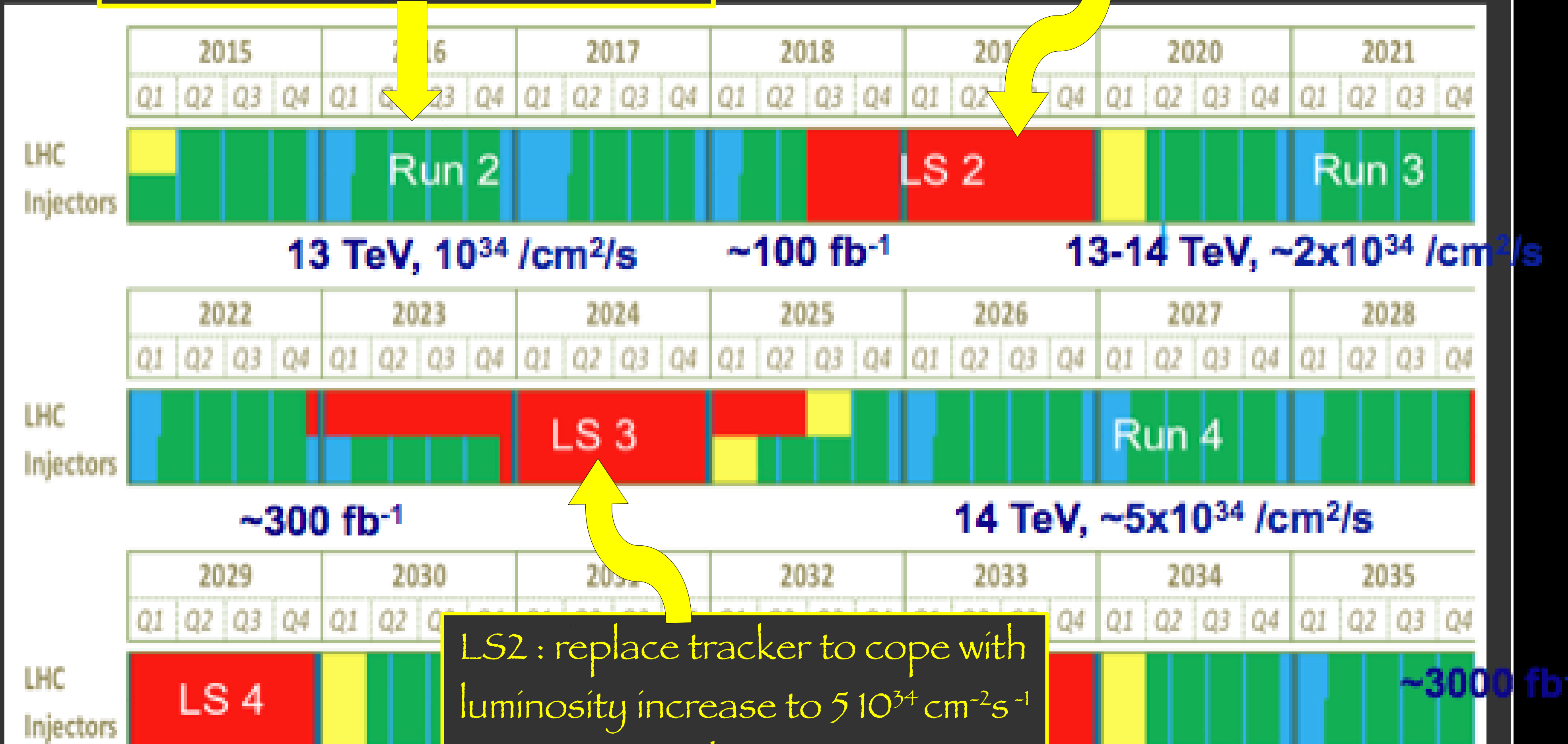
2015 : RUN with smaller beam pipe, useful for next upgrade

LS2 : replace pixels to cope with luminosity increase to 2 10^{34} $cm^{-2}s^{-1}$

Upgrade Plan

2015 : RUN with smaller beam pipe, useful for next upgrade

LS2 : replace pixels to cope with luminosity increase to 2 10^{34} $cm^{-2}s^{-1}$



LS2 : replace tracker to cope with luminosity increase to 5 10^{34} $cm^{-2}s^{-1}$ and ageing

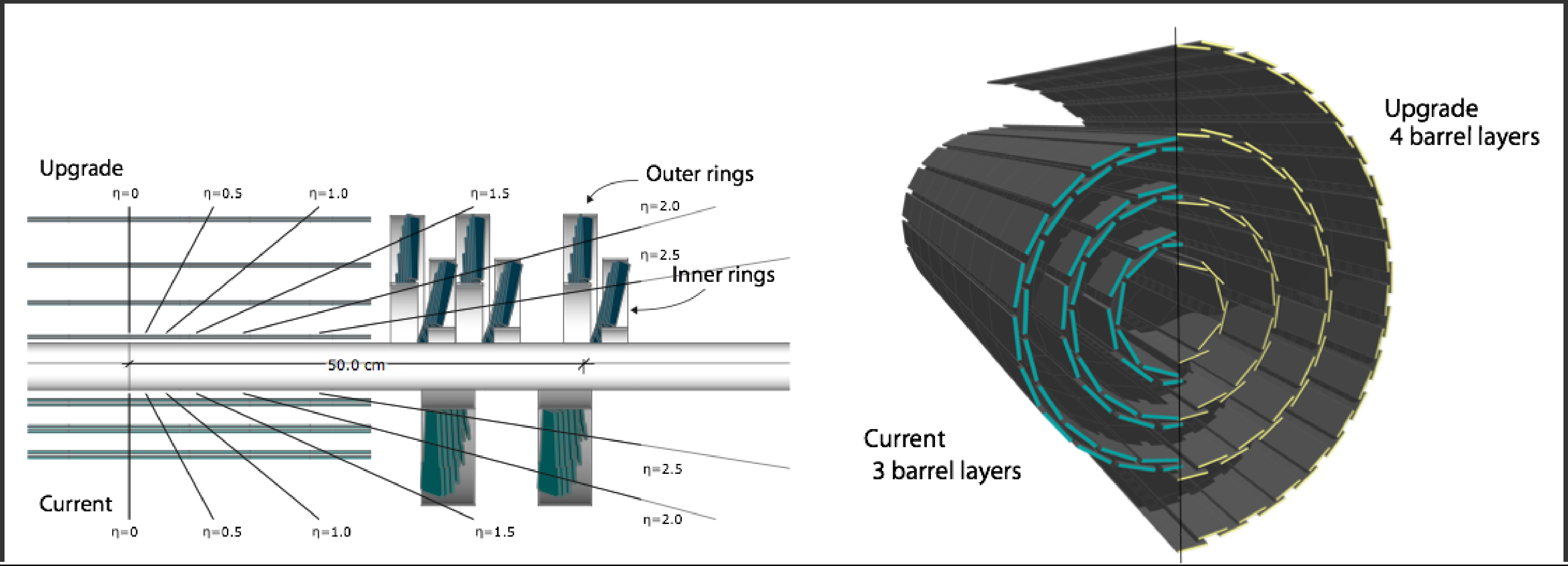
PIXEL Upgrade

- Main features
  - four layers, inner closer to interaction region
  - new readout, reduce data loss
  - new cooling, lighter mechanical support, electronic & connections out of Tk volume
  - overall easier access

Exploit smaller beam pipe
Increase precision and redundancy

Reduce material

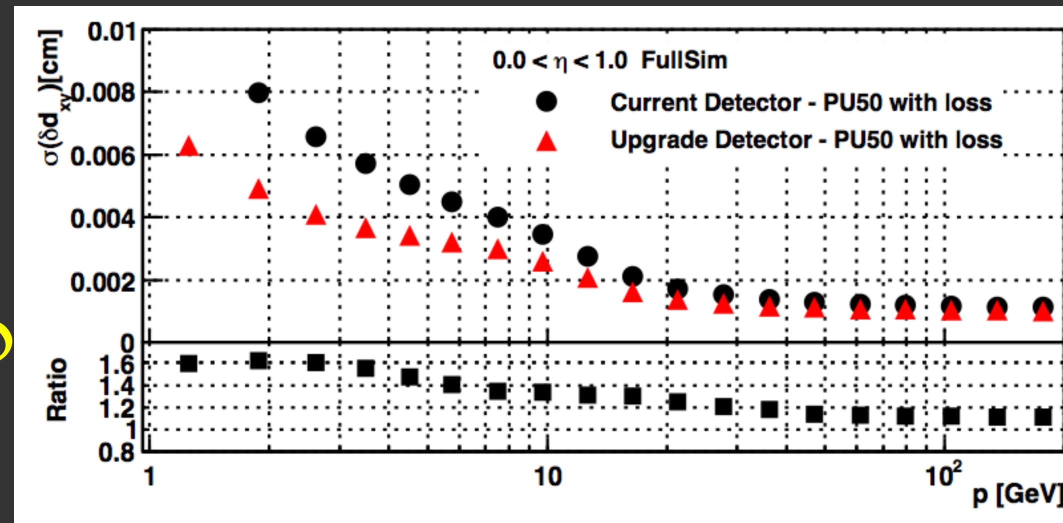
Operation, replacement



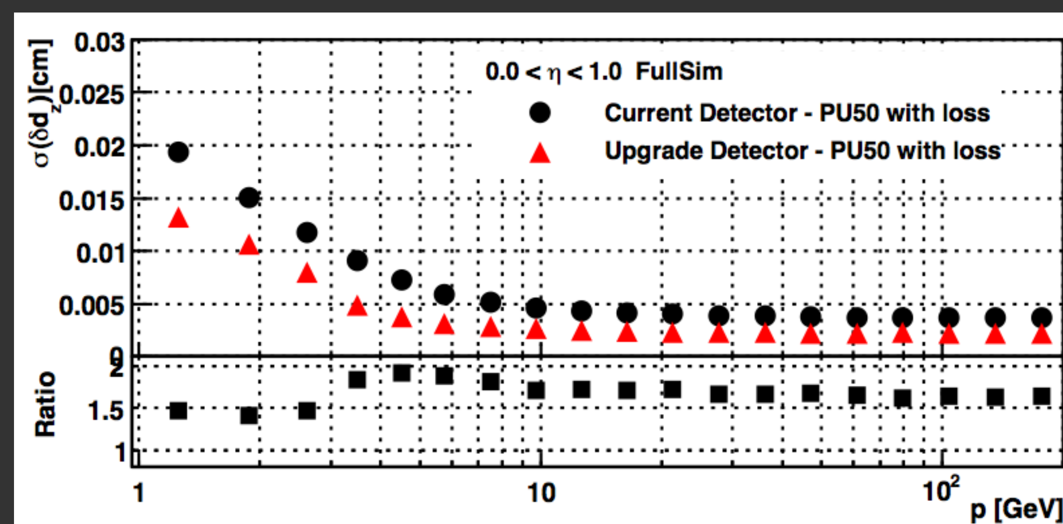
Upgraded Pixel Performance

- Main benefit at low p_T
- Helpful for B-Physics

CERN-LHCC-2012-016



Impact ParameterResolution, *xy*



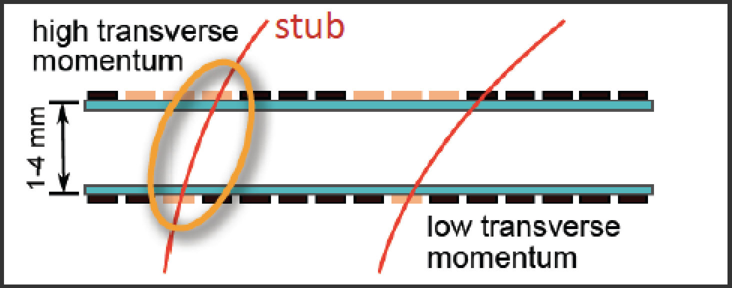
Impact ParameterResolution, *z*

Upgraded Tracking

- Radiation hardness
- Granularity
  - resolve 150-200 collisions per bunch, with few % occupancy
- Reduce material (nuclear interaction, γ conversion)
- Repare modules at short stops
- Provide L1 trigger

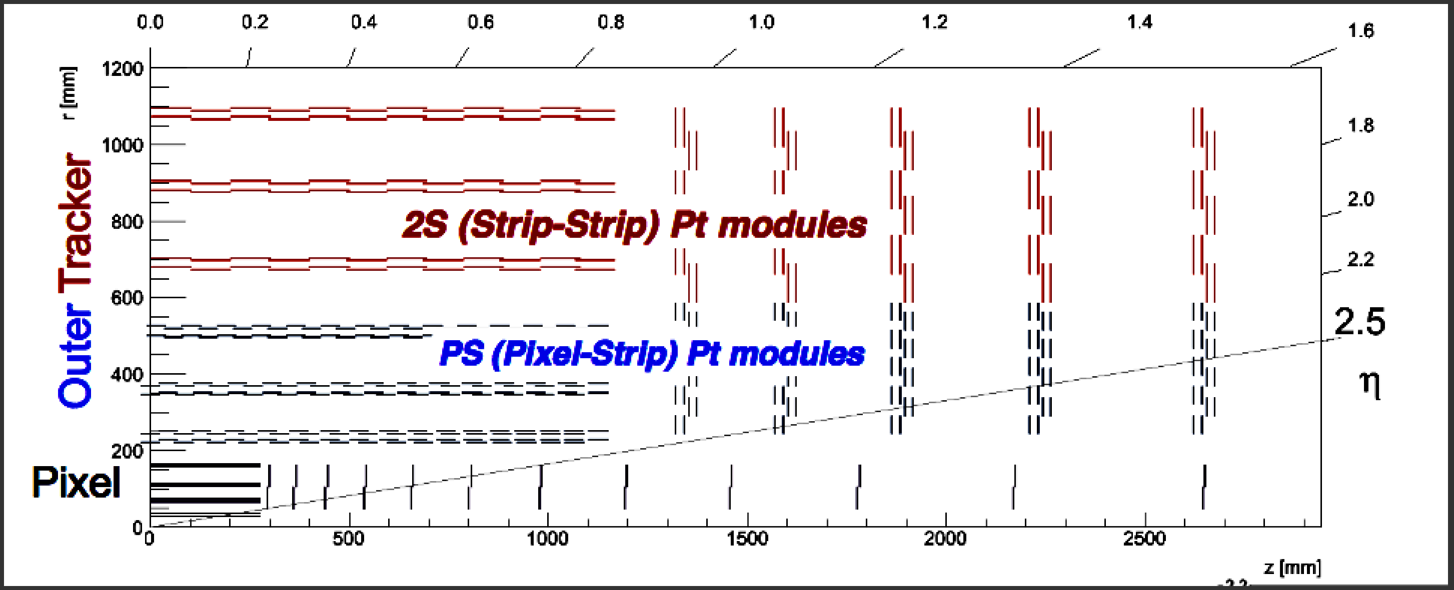
Upgraded Tracking

- Radiation hardness
- Granularity
  - resolve 150-200 collisions per bunch, with few % occupancy
- Reduce material (nuclear interaction, γ conversion)
- Repare modules at short stops
- Provide L1 trigger
- Measure (high) p_T on board the modules:
  - two close modules red-out by one single chip

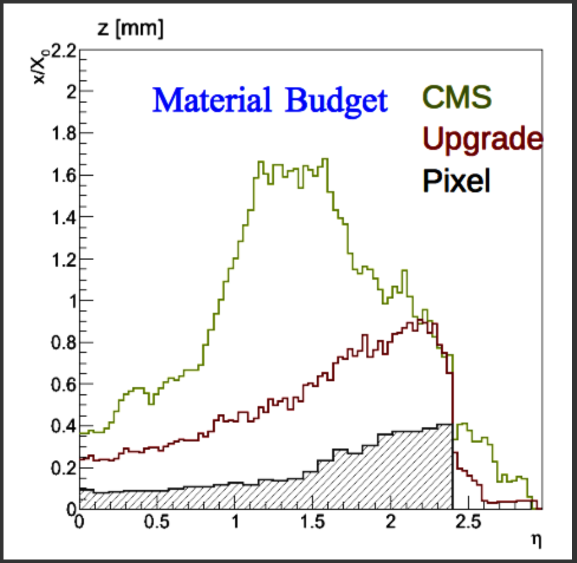


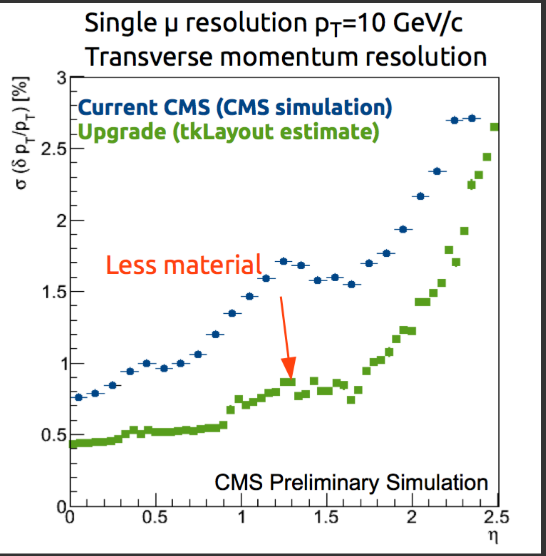
Inner : Pixel+Strip (PS)
Outer : Strip+Strip (2S)

Upgraded Tracker Layout & Performance



- Sizeable reduction of material
- Sizeable Improvement in p_T resolution



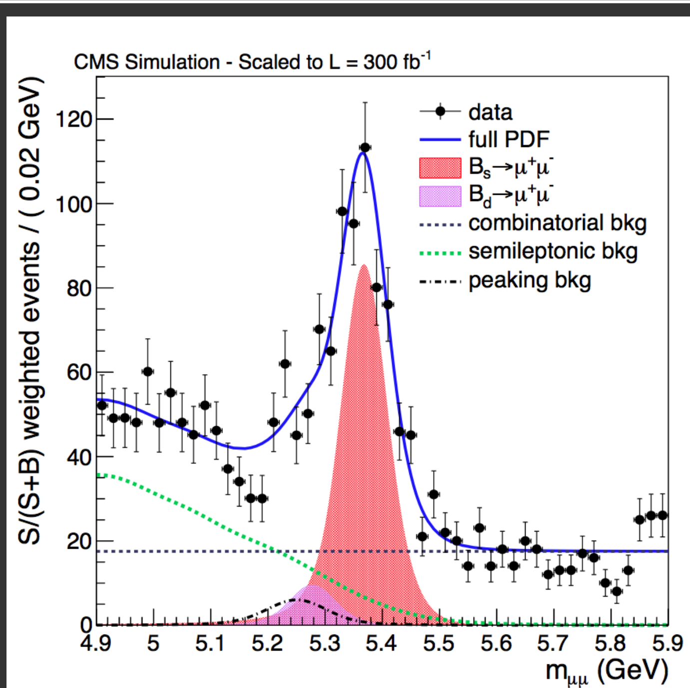


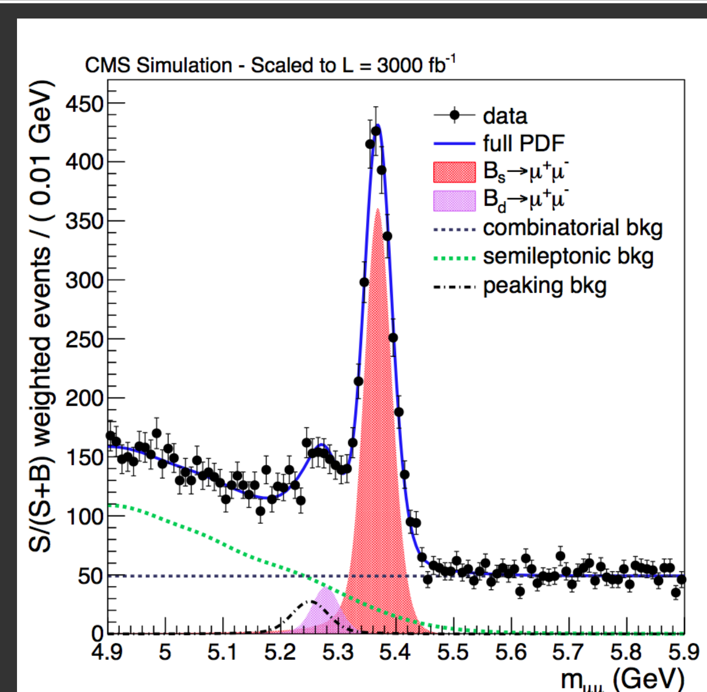
Benchmark : $B \to \mu\mu$

Hypothesis :

- L1 track-Trigger allows same L1 thresholds as now ($p_T(\mu) > 3$ GeV)
- Efficiency :
  - pileup : $\varepsilon(\mu\mu) \downarrow$ 30% (isolation)
  - μ reco & trigger : $\varepsilon(\mu\mu) \downarrow$ 2 x 5%
- σ(syst) :
  - f_s/f_u : 5% (now) → 3%
  - Normalization ($B^+ \to \psi K^+$): $3\%^{(BR)} \oplus 5\% / \sqrt{\mathcal{L}_{INT}/20\ fb^{-1}}$ (Rate)
  - Peaking Backround : $10\%^{(BR)} \oplus 50\% / \sqrt{\mathcal{L}_{INT}/20\ fb^{-1}}$ (Control Sample)
  - Semileptonic Background : $20\%^{(BR)} \oplus 50\% / \sqrt{\mathcal{L}_{INT}/20\ fb^{-1}}$ (Control Sample)
- Resolution:
  - $\downarrow$ 1.6 (Barrell) $\downarrow$ 1.2 (Forward)
  - ignore improvement due to 1st pixel layer

B−>μμ : expectations

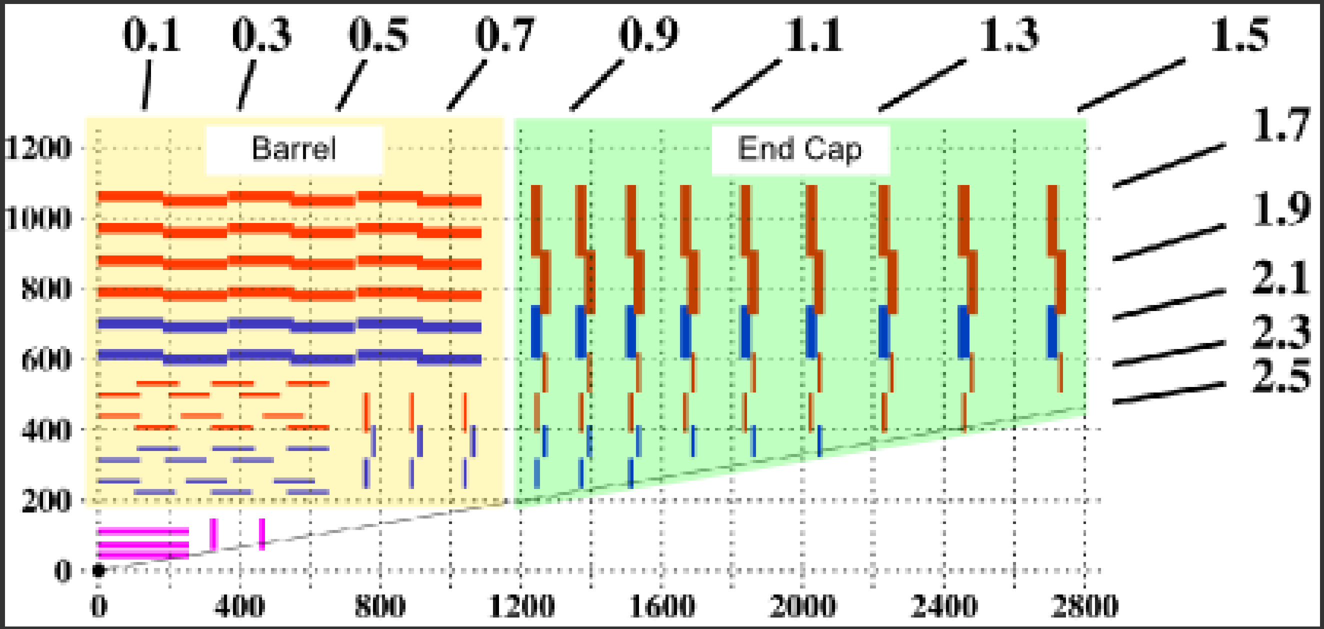




L (fb^{-1})	No. of B_s^0	No. of B^0	$\delta\mathcal{B}/\mathcal{B}(B_s{}^0 \to \mu^+\mu^-)$	$\delta\mathcal{B}/\mathcal{B}(B^0 \to \mu^+\mu^-)$	B^0 sign.	$\delta\frac{\mathcal{B}(B^0\to\mu^+\mu^-)}{\mathcal{B}(B_s^0\to\mu^+\mu^-)}$
20	16.5	2.0	35%	>100%	0.0–1.5 σ	>100%
100	144	18	15%	66%	0.5–2.4 σ	71%
300	433	54	12%	45%	1.3–3.3 σ	47%
3000	2096	256	12%	18%	5.4–7.6 σ	21%

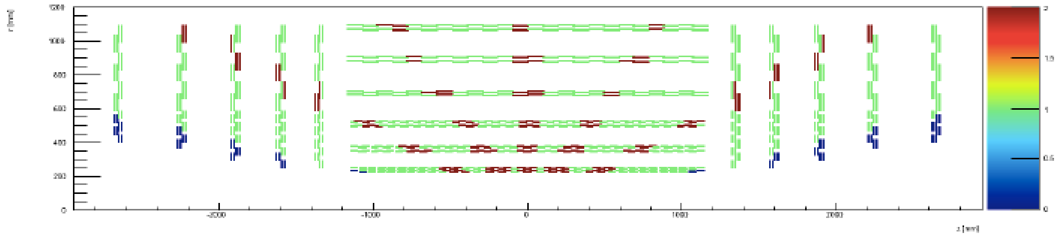
- 3000 fb^{-1} : statistic is not an issue
- Use just barrel events, resolution is enough to separate B_d/B_s/B->hh'
- $\mathcal{B}r$ (B_d) > 5 σ

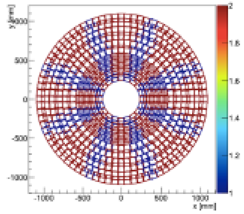
Backup: current tracker layout



Backup : Hardware Track Trigger

- Subdivide tracker into trigger towers
- 8(r-φ)x6(r-z) trigger sectors (some 10% overlapping)
  - Each sector ~200 stubs on average; tails up to ~500 stubs/event in 140 evts pileup+ttbar
    - About 600 Gb/s per one trigger tower





- Send data to Track-finding processors
- Full mesh ATCA shelfs
  - "40G" full-mesh backplane on 14 slots = 7.2 Tb/s
  - time multiplexing data transfer from a set of receiving boards to pattern recognition and track finding engine
  - O(10) time multiplexed at the shelf level